VASAVI COLLEGE OF ENGINEERING *(Autonomous)*, IBRAHIMBAGH, HYDERABAD-31

M.E./M.Tech. (CBCS) I-Semester Main Examinations, Jan.-2018

No.311/CoE/2018

TIME TABLE

Date: 01 -11-2018

Timings: 10.00 am to 1.00 pm

DATE / DAY	E.C.E.		E.E.E.	MECHANICAL	C.S.E.
	Communication Engineering & Signal Processing	**Embedded Systems & VLSI Design**	**Power Systems & Power Electronics**	**Advanced Design & Manufacturing**	
31.12.2018 Monday	English for Research Paper Writing Finishing School-I (Old) (10.00 am to 11.30 am)				
02.01.2019 Wednesday	Advanced Digital Signal Processing	Embedded Systems Design	Advanced Computer Methods in Power Systems	Mathematical Methods for Engineers	Mathematical Foundations of Computer Science
04.01.2019 Friday	Advanced Digital Modulation Techniques	Digital IC Design	Power Electronic Converters	Metal Cutting and Forming	Advanced Data Structures
07.01.2019 Monday	Image and Video Processing	Analog IC Design	Application of Power Electronics to Power Systems	Computer Integrated Design and Manufacturing	Advanced Operating Systems
09.01.2019 Wednesday	Data and Computer Communication Networks	Advanced Computer Organization	Power System Stability	Mechanical Vibrations	Artificial Intelligence
11.01.2019 Friday	Audio and Speech Signal Processing	VLSI Technology	High Voltage DC Transmission	Flexible Manufacturing Systems	Advanced Database
16.01.2019 Wednesday	Adaptive Signal Processing	VLSI Physical Design	Power Quality Engineering	Finite Element Techniques	Information Security

Note: Clash/Omission(s) if any, may be immediately brought to the notice of the undersigned.

Sd/-
Controller of Examinations

Copy to:

1. The Principal, VCE for information.
2. The Director, Admissions and Examinations, VCE. } with a request to bring it to
3. The Head, Department of CSE/ECE/EEE/Mech. Engg./H&SS/Mathematics, VCE. } the notice of all concerned.
4. The Coordinator, Computer Centre, VCE, with a request to upload the timetable in the college website.
5. The Librarian, VCE for information.